REMARKS

Present Status of the Application

The Office Action rejects claims 1-2 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office Action also rejects claims 1-2 under 35 U.S.C. 102(b) as being anticipated by Sherman (US Patent No. 5,784,262).

Upon entry of the amendments in this response, claims 1-2 are amended and remain pending in the present application. Claim 1 is amended by clearing the limitation that is supported by Figs. 2A, 4A, and 5A-5C. Claim 2 is also amended by clearing the limitation that is supported by Figs. 2A and 4A. Applicant believes that the foregoing amendments do not introduce new matter. Thus, reconsideration of those claims is respectfully requested.

Response to Claim Rejections under 35 U.S.C. 112

The Office Action rejects claims 1-2 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claims 1-2 to improve clarity. Accordingly, Applicant respectfully submits that the rejection under 35 U.S.C. 112 has been overcome and should be withdraw.

Response to Claim Rejections under 35 U.S.C. 102(b)

The Office Action also rejects claims 1-2 under 35 U.S.C. 102(b) as being anticipated by Sherman (US Patent No. 5,784,262). Applicant respectfully transverses the rejection as it applies to claims 1-2, as amended, for at least the reasons set forth below.

The independent claim 1, as amended, recites as follows.

1. A standardized circuit board core, comprising:
a dielectric core layer having a first surface and a related second surface, and divided into a plurality of partial areas; and
a plurality of solid conductive posts passing through the dielectric core layer and connecting to the first surface and the second surface of the dielectric core layer, wherein the conductive posts are arranged in an array form in at least one of the partial areas of the dielectric core layer.
(Emphases added)

Apparently, the claim invention provides a standardized circuit board core that has a dielectric core layer and a plurality of *solid* conductive posts. The *solid* conductive posts pass through the *single* dielectric core layer, and are arranged in an array form in a partial area of the *single* dielectric core layer.

Sherman, however, is directed to a multi-layer circuit board or a substrate member (Item 20 in Fig. 1). Sherman disclosed that "Substrate openings, or through-holes, 22a-22d extend from outer side 11a to the other side 11b of base 20. These through-holes, referred to as vias, have been lined with a conductive material shown at 24a-24d." (col. 4 lines 51-54 and Fig. 1). Thus, it is clear that all of these through-holes 24a-24d are hollow, but not solid. Furthermore, Sherman's through-holes 24a-24d pass through three dielectric layers and two circuit layers at a time (see Fig.1), but not pass through a single dielectric layer.

Therefore, Sherman does not anticipate claim 1, as amended, since Sherman does not disclose the *solid* conductive posts and the *single* dielectric core layer of the present invention. Consequently, Sherman does not anticipate claim 2 dependent on claim 1 as a matter of law.

Accordingly, Applicant respectfully submits that the grounds of rejection have been addressed and the rejection has been overcome. Reconsideration and withdrawal of the rejection are respectfully request.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-2 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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